THE MARK-8 USER GROUP IS ALIVE AND RUNNING. IT'S ONLY 14 SEPT. AND WE ALREADY HAVE RECEIVED LETTERS FROM 30 PEOPLE. IT IS QUITE POSSIBLE THAT WE MAY END UP WITH HUNDREDS OF PARTICIPANTS. THIS ISSUE WILL INCLUDE A FEW THINGS THAT SEEM URGENT AND WE'LL SAVE THE GOOD THINGS FOR FUTURE ISSUES AFTER WE ACCUMULATE SOME MORE PARTICIPANTS.

1. HOW DO YOU KEEP FROM PAYING $120 FOR THE 8008 CHIP?
   A. GET A SCHOOL DISCOUNT OF 20% FROM AN INTEL DISTRIBUTOR.
   B. TRY COOK, 25W178-39TH ST., NAPERVILLE, IL 60540 $80 (P. 110 RE OCT)
   C. BEG RGS ELECTRONICS, 3650 CHARLES ST., SUITE K, SANTA CLARA, CA 95050 TO STOCK THEM AGAIN AT $50. I GOT 2 FROM THEM BUT THEY SAY THEY ONLY HAVE ENOUGH LEFT FOR THEIR IK 8008 KIT. SEE P. 102 RE OCT AND 73 MAGAZINE P. 87 JUNE.
   D. TRY BILL GODBOUT ELECTRONICS, BOX 2673, OAKLAND AIRPORT, CA 94614 $50, SEE AD IN 73 MAG. P. 87, JUNE 74.

2. HOW MANY BUGS ARE THERE IN THE CONSTRUCTION ARTICLE?
A FEW HAVE SHOWN UP SO FAR. J. TITUS, THE AUTHOR MENTIONS THESE:
   A. CONNECTIONS ON BOTTOM OF BOARD ARE IN PARALLEL. ARRANGE BOARDS IN ORDER SHOWN IN BOOK AND WIRE. THEN CUT OUT WIRES BETWEEN CONTACTS 9 THRU 16 BETWEEN INPUT MUX AND ADDR/MANUAL BOARDS.
   B. ON PAGE 6, 4TH PARAGRAPH, LAST LINE, IT SHOULD READ "ON THE FOLLOWING INSTALL THE B JUMPERS AND RESISTORS R1-R4 AND R21."

PLEASE REPORT ANY OTHER BUGS OR CONSTRUCTION PROBLEMS YOU FIND.

3. HOW DO YOU REMOVE AN IC FROM THE PC BOARDS WITHOUT REMOVING THE FOIL TOO? I GIVE UP, HOW? EVEN MOLEX IC SOCKET PINS ARE HARD TO USE ON THE MEMORY BOARDS. IF ONLY THE COMPLICATED FOIL PATTERNS COULD HAVE BEEN ON THE BOTTOM SIDE INSTEAD OF THE TOP SIDE OF THE BOARDS.

4. WHAT DO YOU DO IF YOU WANT MORE INPUT PORTS?

A. USE J. TITUS'S BUS IDEA ON PAGE 9 AND 10.

B. REWIRE THE INPUT MUX BOARD AS SHOWN IN FIG. 1 FOR AN INPUT BUS EITHER TRI-STATE OR WIRED-OR.

C. IF YOU NEED MORE THAN 8 INPUT PORTS, TRY THIS. THE AC COMES OUT AT T1 OF MEM CYCLE 2 ON AN INP INSTRUCTION. I BELIEVE IT WILL BE LATCHED INTO IC-8&9. BY INCLUDING THE PROGRAMMING INSTRUCTIONS

```
LAI     (LOAD IMMEDIATE)
15      (DEVICE NUMBER)
INP B   (PORT BEING MULTIPLEXED)
```

AND USING A 7442 OR 74154 TO DECODE THE AC INFO, YOU CAN HAVE AS MANY INPUT PORTS AS YOU WANT. (MORE ABOUT THIS IN A FUTURE ISSUE.)

5. HOW DO I CONNECT A TELETYPE? A SCHEMATIC IS SHOWN IN FIG. 2.

6. HOW DO I BUILD A MODEM FOR A CASSETTE RECORDER? A GOOD QUESTION. HERE ARE TWO UNTRIED PARTIAL CIRCUITS I'VE FOUND. IF ANYONE HAS BETTER INFORMATION, PLEASE GET IT TO US SO WE CAN DISTRIBUTE IT. THIS SEEMS TO BE EVERYONE'S TOP PRIORITY PERIPHERAL.

7. HOW CAN I GET HELP OR MORE INFORMATION ON CONSTRUCTING MY MARK-8 OR HELP IN DEBUGGING? HEAD OUT TO THE NEAREST ENGINEERING COLLEGE. EVERY ONE HAS A WHOLE BUNCH OF MICROPROCESSOR PROJECTS GOING ON AND CAN PROBABLY HELP YOU OUT WITH DEBUGGING, SOFTWARE, AND ROM PROGRAMMING, ETC. LET THE REST OF US KNOW WHAT YOU FIND OUT.

8. WHAT HAVE THE PARTICIPANTS SAID SO FAR?
JIM FRY IS DEVELOPING A CURSOR BOARD FOR TV TYPEWRITER WITH PROGRAMMABLE CURSOR CONTROL AND IS TRYING TO IMPLEMENT AN ELABORATE INTERRUPT CAPABILITY.

GREG HUNTZINGER IS GOING TO USE THE MICRO-8 AND TV TYPEWRITER AS A TV TITLING SYSTEM FOR TV TAPING AND FOR COMPUTER ART.

ROBERT KELLY HAS 2 BAUDOT TTY'S HE WANTS INFO ON USING.
K. A. MCGINNIS WANTS TO OBTAIN CHEAP WIRE WRAP SOCKETS. HE ALSO WANTS TO KNOW IF ANYONE IS INTERESTED IN BUILDING 8080 BASED COMPUTERS. I AM IS ANYONE ELSE?

LAURENCE PLATE IS READY TO WRITE A BASIC AND WANTS TO INTERFACE A TRIG CALCULATOR

TERRY RITTER IS THE FIRST ONE TO SAY HIS MARK-8 IS RUNNING AND HAS SOME NEAT IDEAS ON PERIPHERALS.

LEE SORENSEN SAYS THE SCELBI-8H USER MANUAL (P. 101 RE OCT 74) IS VERY VALUABLE.

JONATHAN TITUS, THE MARK-8 AUTHOR IS GOING TO CONTRIBUTE INFO ON A REMOTE INTERRUPT MODULE AND A 2102 RAM MEMORY . HE ALSO TELLS US THAT HE HAS A CALCULATOR INTERFACE ARTICLE SCHEDULED FOR RE IN THE NEXT COUPLE OF MONTHS.

9. WHAT IS THE CABRILLO COMPUTER CENTER? WE ARE THE EDUCATIONAL COMPUTER INSTALLATION FOR CABRILLO HIGH SCHOOL. WE PRESENTTLY HAVE A 4K PDP8/E WITH A 32K DISK, OPTICAL MARK SENSE CARD READER, 2 TTY'S, A CENTRONICS 508 LINE PRINTER (DUE ANY DAY), A HOMEMADE PAPER TAPE READER AND PUNCH, HOMEMADE OSCILLOSCOPE GRAPHICS TERMINAL, AND A HOMEMADE SWITCH RELAY INTERFACE. WE WILL SOON BE EXPANDING TO A PDP-8/E ETOS 6 USER MULTILANGUAGE OS-8 TIME SHARE SYSTEM. WE WILL HAVE A COUPLE OF HOMEMADE 8008 SYSTEMS RUNNING SOON AND THE EE DEPARTMENT AT UNIV OF CA AT SANTA BARBARA IS INVESTIGATING THE POSSIBILITY OF LOANING US ONE OF THEIR VERY ELABORATE 8008 TRAINING SYSTEMS FOR EVALUATION IN THE HIGH SCHOOL ENVIRONMENT.
10. WHAT CAN WE EXPECT FROM THE NEWSLETTER IN THE FUTURE? NOTHING!!! UNLESS YOU ARE WILLING TO CONTRIBUTE. I AM WORKING ON: 1) OBTAINING INFO ON SOFTWARE SOURCES. 2) GETTING PERMISSION TO RELEASE A BUNCH OF INFO FROM LAWRENCE RADIATION LABS. 3) A CONSTRUCTION ARTICLE ON MY SPECIALITY, $75 HIGH SPEED PAPER TAPE READERS 4) A CONSTRUCTION ARTICLE ON A SCOPE GRAPHICS TERMINAL. WE NEED BADLY: 1) MODEM INFO FOR CASSETTE RECORDERS. 2) SOURCES OF TTY'S CHEAP. 3) INFO ON THE RELIABILITY OF VARIOUS DISCOUNT IC SUPPLIERS. 4) CIRCUITS FOR CONVERTING BAUDOT TO ASCII AND VICE VERSA FOR CHEAP TTY'S. 5) MODIFICATIONS TO TV TYPEWRITER TO INCLUDE SCHROLLING. PLEASE CONTRIBUTE A FEW MINUTES OF YOUR TIME TO SEND IN ANYTHING THAT OTHER BUILDERS MIGHT BE INTERESTED IN. DON'T LET THIS NEWSLETTER DIE LIKE SO MANY OTHERS HAVE BECAUSE OF THE PARTICIPANTS RELUCTANCE TO CONTRIBUTE.

GOOD LUCK IN DEBUGGING AND MAY YOUR SOLDER BRIDGES BE FEW AND FAR BETWEEN.
KEEP THOSE CARDS AND LETTERS COMING IN.

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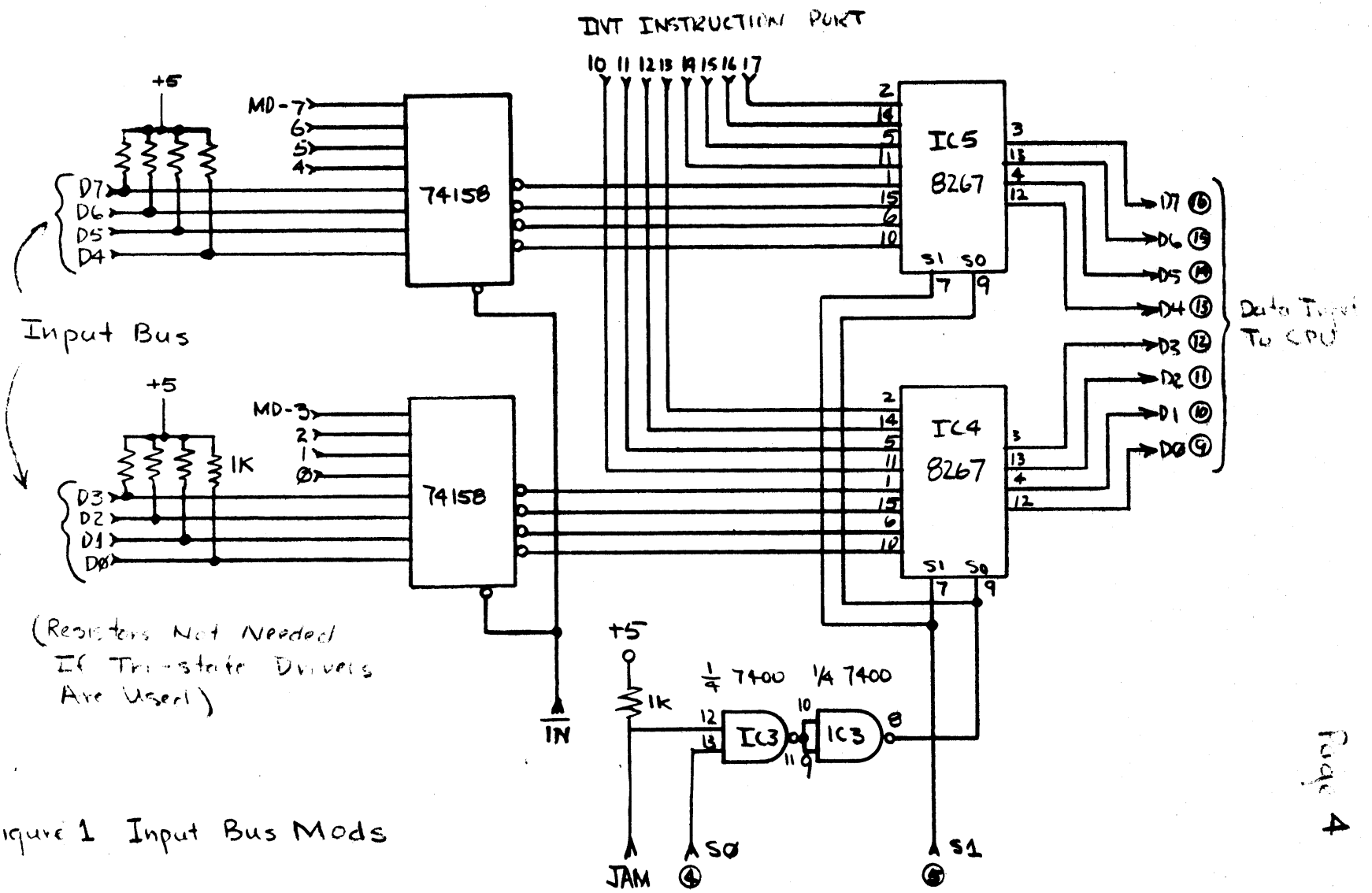


Figure 1 Input Bus Mods

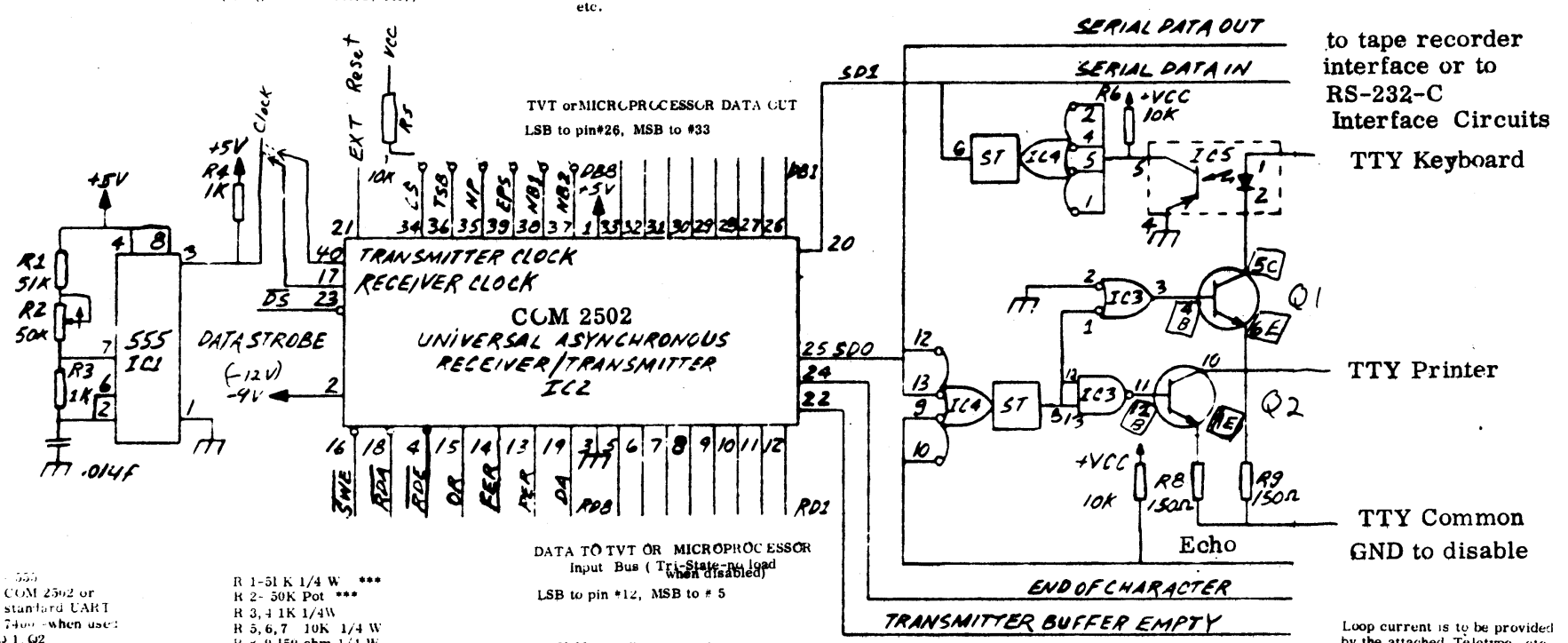
Figure 2 TTY Connection

Pin # 36 L One Stop Bit H Two Stop Bits	No. of Data Bits	5 #37L, #38L 6 #37L, #38 H 7 #37H, #38L 8 #37H, # 39H	PARITY #35 H No Parity #39 L Odd Parity #39 H Even Parity

Connect pins to Gnd for L; to VCC for H, through 10K, R-5
(Hardwire, use on board switchs, bring to control panel direct, or use gates)

ADDITIONAL IC's MIGHT BE NEEDED TO CUSTOMIZE UART CIRCUIT TO INDIVIDUAL NEEDS (OR gates, inverters, etc.)

#23 Transmitter Data Strobe - L enters data into transmitter buffer- such as keyboard strobe, processor output port strobe, etc.



IC 1 - 555
IC 2 - COM 2502 or other standard UART
IC 3 - 7400 when used with Q 1, Q2 Otherwise 75450
IC 4 - 74L Optional
IC 5 - 555 (for a second clock rate)
IC 6 - 7400 /7408 if added gating or inversion desired
Q 1, 2 - 2N3643 or 2N2222 or other NPN
(12B, 10C, 9E, etc. refers either to pin number on 75450 or base, collector, and emitter of transistor.)

R 1-51 K 1/4 W ***
R 2- 50K Pot ***
R 3, 4 1K 1/4W
R 5, 6, 7 10K 1/4 W
R 8, 9 150 ohm 1/4 W

C 1 - 2.1mfd 25-50V (bypass across both power supplies)
C 2 .01 timing cap ***
C4, 5, 6, 7 .01 discs
(across VCC-GND at each IC)
*** Change if needed for higher Baud rates.

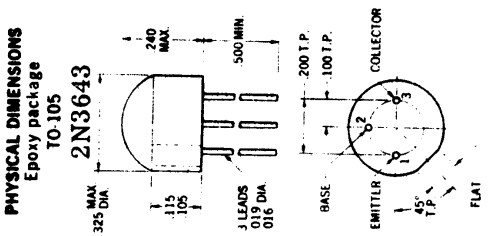
#21 Master Reset, needs to be pulsed high after system turn on(to be controled by system initialize)
#19 RDA, (Tri-state) is H when data is avavailable at receiver(#5- #12)
#18 RDAR a L clears the RDA flag
#4 RDE when brought to L, enables tri-state output of Receiver, #5-#12
#13, #14, #15 are error flags (for visual indicators, or software messages to processor)
#16 When at L, enables above, RDA, TMBT, and would normally be tied to ground

*NOTE- Normal supply voltages, VCC, #1, 5V, VDD, #2, -12V, Gnd, #3. VDD may be -9 if Baud rate doesn't exceed 10K (normal uses it won't) and strobes are in the order of 1 us.

Baud rate should be adjusted to 16 X

Clock rate (output of 555, pin #3) should be adjusted to 16 X the desired Baud rate, and is connected to UART pins #17, #40 if the receiver and transmitter are to be operated at the same Baud rate. Of course, if additional Baud rates are desire arrange for additional 555's or to switch timing components.

Loop current is to be provided by the attached Teletype, etc.



FSK DATA CONVERTER FOR CASSETTE RECORDER

A circuit scheme which allows an ordinary reel or cassette tape recorder to be used as a digital data recorder was submitted by Daniel Chin of Burlington, Massachusetts.

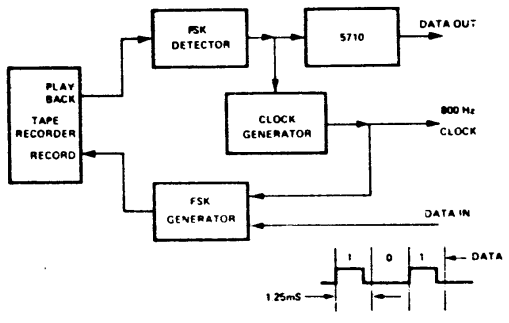
"The circuit design allows any single-track audio tape recorder with frequency response to 7kHz to be used as a digital recorder for many non-critical applications. This application provides a complete data recording system using two recorded frequencies on a single track. The two frequencies are obtained from two synchronized NE565s. Detection of the recorded frequencies requires a third NE565. A fourth circuit is used to generate and synchronize the system clock. The advantages obtained by using these techniques are elimination of the need for:

1. A timing channel to strobe off the data, or
2. A third frequency for null, while using the other two frequencies for 1 and 0.

This implementation, therefore, is one of the simplest ways to get a digital recording system on an audio recorder. It is shown in block diagram form in Figure 8–75.

The parameters chosen for the circuit design allow a digital recording bit rate of 800Hz or 100 8-bit characters per second. Though 100 characters per second is less than the 300-character-per-second speed of a high-speed paper tape reader, the low cost of this circuitry combined with the audio tape recorder should make this system very attractive from a cost performance viewpoint. This is especially true when compared with the normal Teletype speed of 10 characters per second.

BLOCK DIAGRAM OF PLL CASSETTE RECORDER



The circuits will also work with the readily available low cost cassette recorders now available, which make compact as well as low cost information storage. A FSK system of recording is used, which allows the voice recording and reproduction electronics of the recorder to be unmodified for use in recording digital information. The retained electronics may also be used to record voice message identification of the various sections of the tape.

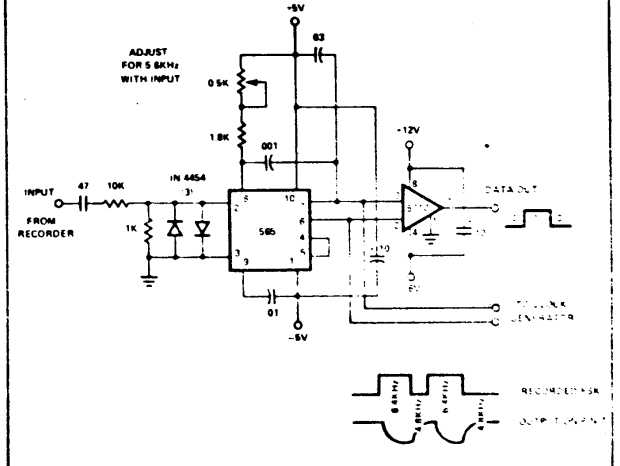
The intended use of this circuit is to convert an audio recorder for minicomputer programs written for engineering design applications. Such an application requires good information storage and retrieval over a wide range of storage time. Redundancy may be incorporated by using a two-channel recorder (stereo) and a FSK detector per channel. The outputs of the two detectors could then be ORed digitally to recovered recorded 1s and, thus, give a safeguard against dropouts.

Circuit Description

Four NE565s are used in three circuits to achieve the design. These are:

The FSK detector (Figure 8–76a) is used to detect 6.4kHz for a 1 and 4.8kHz for a 0. The data output is taken from a 5711 connected to pins 7 and 6 of the NE565. The recording method used is RZ FSK, which means that a zero is recorded as 4.8kHz for the entire bit period and one is recorded as 6.4kHz for about 60 percent of the period and 4.8kHz for the remaining 40 percent of the period. This 60 percent bit duty cycle insures that the clock will synchronize with a negative transition during the time that a 1 should be detected.

CASSETTE RECORDER FSK DETECTOR, CLOCK GENERATOR AND FSK GENERATOR



PHASE LOCKED LOOP APPLICATIONS

The clock generator (Figure 8–76b) is used to derive the 800Hz with no input. When the data pulses are extracted from the recorded data, the clock is synchronized to the data. The design allows up to 7 zeros in succession without causing the clock to go out of synchronization. This condition is easily met if odd parity is used to record the 8-bit characters. (One of the 8 bits is a parity bit and, thus, one bit out of 8 is always a one.)

The FSK generator (Figure 8–76c) provides the FSK signal for recording on tape. It consists of 2 oscillators locked to the basic 800Hz system clock but oscillating at 6.4kHz and 4.8kHz. The incoming data to be recorded selects either oscillator as the frequency to be recorded. Harmonic suppression of the square wave output is taken care of automatically by the high frequency roll off characteristic of the tape recorder."

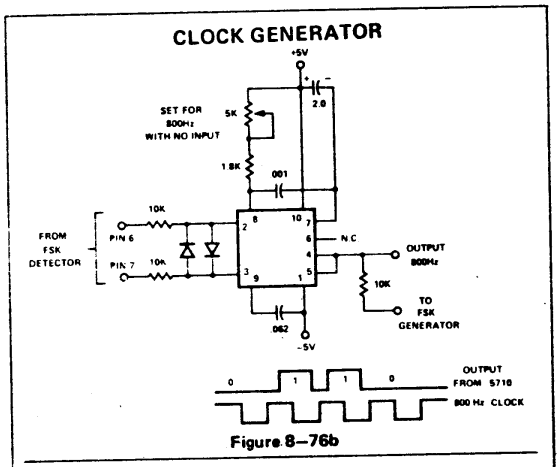


Figure 8–76b

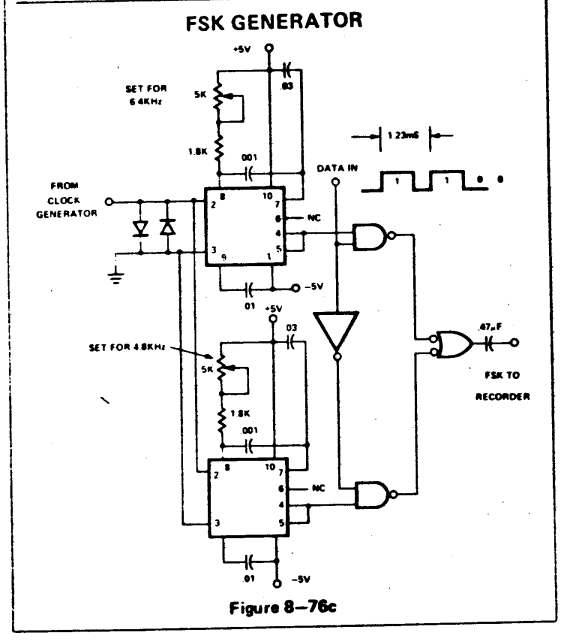


Figure 8–76c

filter is formed by connecting a capacitor or an RC network from pin 2 to ground, as shown in Figure 16. The resulting filter transfer functions are also shown in the figure where R_1 (= 6 kΩ) is the internal impedance at pin 2. In this application, pin 3 is ac grounded through a bypass capacitor, C_B, to insure proper ac bypass ($C_B \geq 10\ C_1$).

In high frequency applications ($f_O > 100$ kHz) for FM demodulation, tone detection and frequency synthesis, it is recommended that pin 3 not be bypassed but connected to ground through a low-pass filter identical to that used at pin 2 (See Figures 22 and 23).

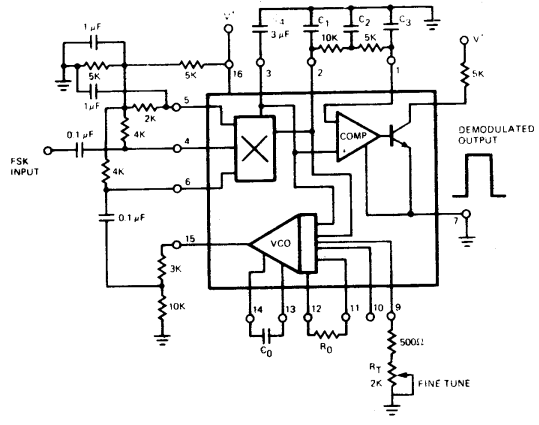


Figure 17. Circuit Connection For FSK Demodulation (Single Supply)

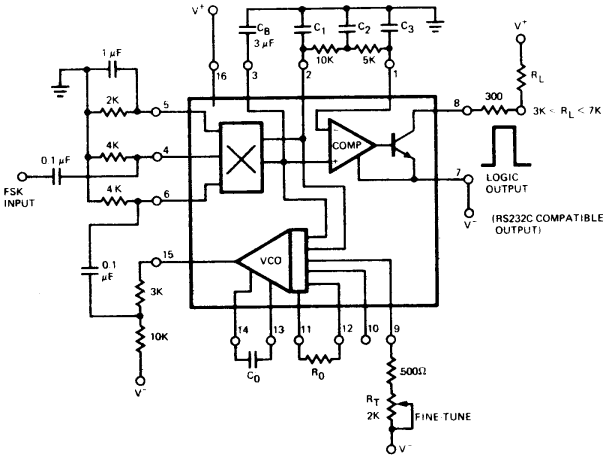


Figure 18. Split-Supply FSK Demodulation with RS232C Compatible Output

APPLICATIONS INFORMATION

FSK DEMODULATION

Figures 17 and 18 show a generalized circuit connection for FSK demodulation. The circuit is connected as a PLL system by ac coupling the VCO output (pin 15) to pin 6. The FSK input is applied to pin 4. When the input frequency is shifted, corresponding to a data bit, the polarity of the dc voltage across the phase detector outputs (pins 2 and 3) is reversed. The voltage comparator and the logic driver section convert this dc level shift to a binary pulse. One of the phase detector outputs (pin 3) is ac grounded and serves as the bias reference for the voltage comparator section. Capacitor C_1 serves as the PLL

loop filter, and C_2 and C_3 as post-detection filters. The timing capacitor, C_0, and the fine-tune adjustments are used to set the VCO frequency, f_o, midway between the "mark" and "space" frequencies of the input signal. Typical component values for 300 baud (103-type) and 1200 baud (202-type) MODEM applications are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070 Hz	R_0 = 5.1 kΩ, C_0 = 0.22 μF
f_2 = 1270 Hz	$C_1 = C_2$ = 0.047 μF,
	C_3 = 0.033 μF, C_4 = 3 μF
High Band: f_1 = 2025 Hz	R_0 = 8.2 kΩ, C_0 = 0.1 μF
f_2 = 2225 Hz	$C_1 = C_2 = C_3$ = 0.033 μF
1200 Baud	R_0 = 2 kΩ, C_0 = 0.14 μF
f_1 = 1200 Hz	C_1 = 0.033 μF, C_3 = 0.02 μF
f_2 = 2200 Hz	C_2 = 0.01 μF, C_4 = 0.1 μF

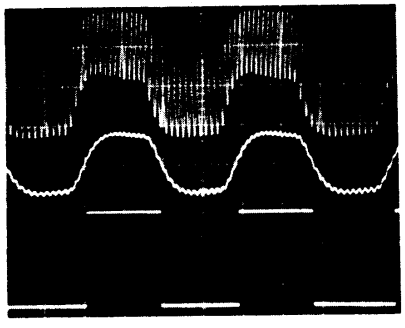


Figure 19. Demodulated Waveforms for 150 Baud Data Rate, f_1 = 1070 Hz, f_2 = 1270 Hz

Top: Pin 2 } 0.5 V/div.
Center: Pin 1 }
Bottom: Pin 8 5.0V/div.

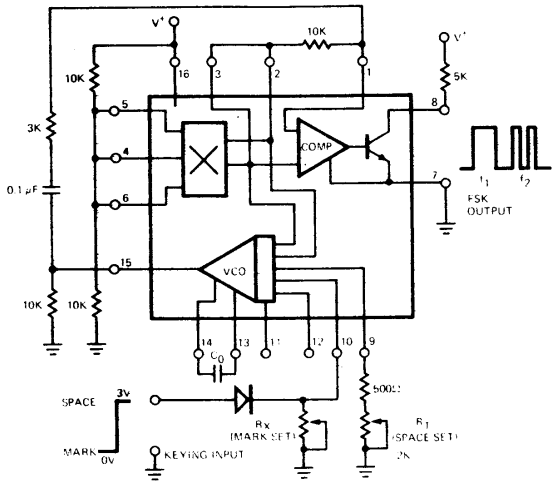


Figure 20. Circuit Connection For FSK Generation (<100kHz)

Figure 19 shows typical waveforms at different points in the circuit for a 150 baud data rate with "mark" and "space" frequencies of 1270 and 1070 Hz respectively. The top waveform is the phase detector output at pin 2; the middle waveform is the filtered signal at the comparator input (pin 1), and the bottom waveform is the logic output at pin 8.

RS-232C COMPATIBLE OPERATION (See Figure 18): For split-supply operation, the logic output section can function as a line-driver circuit, compatible with RS-232C specifications. This can be achieved by connecting a 300Ω series resistance to pin 8, and choosing a pull-up resistor R_L in the range of 3 KΩ to 7 KΩ.

ENABLE/DISABLE CONTROLS: In FSK demodulation applications, the operation of the circuit can be "inhibited" by applying a disable logic signal to either pins 2, 3 or 5. Application of a ***negative*** inhibit pulse to pin 3 introduces a dc offset across the comparator inputs and sets the logic output (pin 8) to a "high" state. If the same pulse is applied to pin 2, then a "low" state occurs at pin 8. Applying either a 3-volt *positive* or *negative* "inhibit" pulse to pin 5 disables the phase detector section, and sets the logic output to a "low" state. The enable/disable controls are particularly useful when using the XR-210 in a carrier-level detection system. Here the circuit can be activated only when the input signal exceeds a pre-set threshold value.

FSK GENERATION

A typical circuit connection for this application is shown in Figure 20. The coarse setting of the frequency is determined by the choice of C_0 across pins 13 and 14. Normally, C_0 is chosen to give a free running frequency, f_o, approximately 5% lower than the "space" frequency, f_1. Then, the "space" and "mark" frequencies f_1 and f_2 are set by the choice of resistors R_T and R_X as:

$$f_1 = f_{space} = f_0\left(1 + \frac{0.1}{R_T}\right) \quad \text{Hz}$$

$$f_2 = f_{mark} = f_1\left(1 + \frac{0.3}{R_X}\right) \quad \text{Hz}$$

where the resistor values are in kΩ. "Space" frequency is set prior to the "mark" frequency with the selection of C_0 and the fine-tune resistor, R_T, with pin 10 open circuited. "Mark" frequency is then determined by the appropriate choice of R_X from pin 10 to ground.

The VCO output available at pin 15 is a symmetrical square-wave with a 2.5 V_{p-p} output amplitude. The duty cycle asymetry of the VCO output is typically less than 2%.

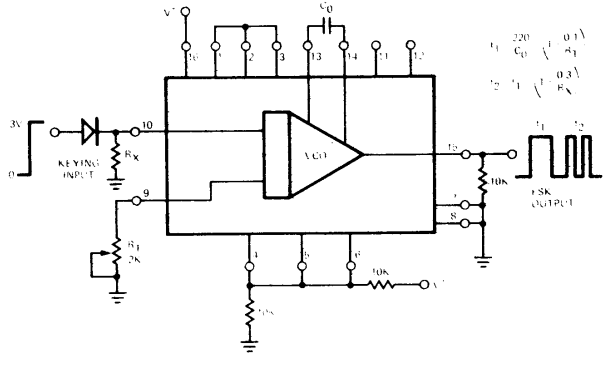


Figure 21. High Frequency FSK Generation Using VCO Section Only